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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/581,873	06/05/2006	Tim Niggemeier	PD030127	3929

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EXAMINER	
GIARDINO JR, MARK A	

ART UNIT	PAPER NUMBER
2185	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/581,873	NIGGEMEIER ET AL.	
	Examiner	Art Unit	
	MARK A. GIARDINO JR	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 December 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

The Examiner acknowledges the applicant's submission of the amendment dated 11/13/2009. At this point, claims 1-5 and 13 have been amended. Thus, claims 1-14 are pending in the instant application.

The instant application having Application No. 10/581,873 has a total of 14 claims pending in the application, there are 2 independent claims and 12 dependent claims, all of which are ready for examination by the examiner.

REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 3-6, 10, 13, and 14 are rejected under 35 U.S.C. 102(b) as being anticipated by Novak et al (US 6,496,906).

Regarding Claim 1, Novak teaches a method for communication between an IC **(CPU 30 of Figure 1)** and an external RAM **(SDRAM 70 of Figure 1)**, where the external RAM has at least one memory bank **(made clear on Column 7 Lines 40-42)** and communication between the IC and the external RAM is performed via two or more channels **(the channels corresponding to the busses from the queues, such as AQ 340, 350, and 360 of Figure 2)**, where data exchange between the IC and the external

RAM necessitates at least two memory bank commands **(Column 2 Lines 26-28, where the commands are activate, read/write, and precharge)**, the method comprising:

transmitting the at least two memory bank commands via multiple channels **(the commands are clearly transmitted through the channels to SDRAM 70 as can be seen on Figure 2)**;

prioritizing the at least two transmitted memory bank commands the basis of a static priority allocation **(the priority is "PQ 350 entries marked hi priority take precedence over RWQ 360 entries [read/write commands] which take priority over AQ 340 entries [activate commands] which take priority over normal PQ 350 [precharge commands] entries", Column 9 Lines 1-5, also see Column 7 Lines 43-50 for explanation of the queues);**

and further prioritizing the at least two commands having the same static priority on the basis of a dynamic priority allocation for the channels **(the read/write queue contains multiple commands with the same priority, Column 7 Lines 59-61, and the first-in-first out structure of the queue is dynamic, as the priority is based on which command came first)**.

Regarding Claim 3, Novak teaches all limitations of Claim 1, wherein the prioritizing the commands having the same static priority on the basis of a dynamic priority allocation for the channels includes:

giving the lowest priority to a channel via which a command has been sent (when a command is sent via the PQ channel, the channel it is on is given the lowest priority, Column 9 Lines 1-5).

Regarding Claim 4, Novak teaches all limitations of Claim 1, wherein the prioritizing the commands having the same static priority on the basis of a dynamic priority allocation for the channels includes:

giving one of the channels the highest priority in the next clock cycle if this channel does not have the highest priority in the current clock cycle and a command is sent via another channel (a command in the PQ and its corresponding channel is given highest priority if it is marked hi priority, so if a command is sent via another channel and a hi priority request is sent via the PQ channel, the PQ channel is granted the highest priority, Column 9 Lines 1-5).

Regarding Claim 5, Novak teaches all limitations of Claim 1, wherein the prioritizing the at least two commands having the same static priority on the basis of a dynamic priority allocation for the channels includes:

withdrawing the highest priority of a channel only when this channel can send a command (when a precharge command that is not flagged as hi priority comes after a precharge command flagged as hi priority, the highest priority of the channel is withdrawn, Column 9 Lines 1-5).

Regarding Claim 6, Novak teaches all limitations of Claim 1, wherein the method further includes accessing physically separate memory areas in the external RAM via the channels (physically separate areas of the memory are clearly accessed,

as the RAM is made up of multiple banks as made clear on Column 7 Lines 40-42, which are physically separate areas).

Regarding Claim 10, Novak teaches all limitations of Claim 1, wherein the method further includes permitting two successive access operations to a memory bank when the access operations are made to the same row in the memory bank (Column 6 Lines 42-49).

Claim 13 is the memory controller with the same limitations as Claim 1, and is rejected under similar rationale.

Claim 14 is the appliance for reading and/or writing to storage media with the same limitations of Claim 1, and is rejected under similar rationale.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Novak in view of Kirsch (GB 2,396,442).

Regarding Claim 2, Novak teaches all limitations of Claim 1 as described above. In addition, Novak teaches a 'Read' or 'Write' command with the second highest priority,

an 'Activate' command with the third highest priority, and a 'Precharge' command the lowest priority (Column 9 Lines 1-5).

However, Novak does not teach giving a 'Burst Terminate' command the highest priority. Kirsch teaches a burst terminate command takes precedence over write and read commands (see how the burst terminate command resets the state machine to the active state in Figure 7, also see Page 13 Lines 30-31 in Kirsch). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to which the subject matter pertains to have implemented the burst terminate command as the highest priority command in the device of Novak. This would be useful when a separate read or write request must be taken care of while the memory is in the middle of a lengthy burst.

Claims 7 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Novak in view of Wheeler et al (US 6,983,350).

Regarding Claim 7, Novak teaches all limitations of Claim 1 as described above.

However, Novak does not teach accessing jointly used memory areas in the external RAM via the channels and the assurance is given that no successive access operations to a jointly used memory area will arise.

Wheeler teaches alternating memory banks such that no successive access operation accesses a jointly used memory bank (Column 5 Lines 33 to 42 in Wheeler). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to which the subject matter pertains to arrange memory operations

in such a way in the device of Novak. Wheeler provides the motivation when he states that the bandwidth of the RAM is improved (Column 5 Lines 40-42 in Wheeler).

Regarding Claim 9, Novak teaches all limitations of Claim 1 as described above. However, Novak does not teach wherein the method further includes always having an access operation to another memory bank effected between two access operations to a memory bank. Wheeler teaches alternating memory banks (Column 5 Lines 33 to 42 in Wheeler, alternating between an even and odd memory bank places at least one access operation between each bank).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to which the subject matter pertains to arrange memory operations in such a way in the device of Novak. Wheeler provides the motivation when he states that the bandwidth of the RAM is improved (Column 5 Lines 40-42 in Wheeler).

Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Novak in view of Chen et al (US 2003/0051108).

Novak all limitations of Claim 1 as described above. However, Novak does not teach wherein the method further includes accessing various memory banks via at least one channel by a network. Chen teaches a network (Bank Usage Sorter 110 in Chen) that allows the channels to access any memory bank (paragraph 0014, also see Figure 3 in Chen). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to which the subject matter pertains to have used this network

to distribute the memory data evenly across the banks because this reduces costs (see Paragraph 0015 in Chen).

Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Novak in view of LaBerge (US 2001/0044885).

Novak teaches all limitations of Claim 1 as described above. However, Novak is silent on depicting the states of the memory banks by associated state machines. LaBerge teaches a memory bank that has a state machine (containing at least the states 'idle' and 'not idle', see Paragraph 0023 and Figure 8 in LaBerge). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to which the subject matter pertains to have used a state machine to control the memory banks because tracking idle states results in reducing latency incurred between successive memory operations (see Paragraph 0019 in LaBerge).

Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Novak in view of the power point entitled "Random Access Memory".

Novak teaches all limitations of Claim 1 as described above. However, Novak does not teach further including a plurality of RAM modules and transmitting a chip enable signal in order to select the desired module. "Random Access Memory" teaches combining several RAM modules into a single RAM module and a chip enable signal (called chip select in the power point) to select the desired module (see Slides 17 and 18). It would have been obvious to a person of ordinary skill in the art at the time the

invention was made to which the subject matter pertains to have combined the RAM modules this way because it allows for larger memories to be made (see Slide 18 in "Random Access Memory").

ARGUMENTS CONCERNING PRIOR ART REJECTIONS

Rejections - USC 102/103

Applicant's arguments with respect to claim 1 and 13 that Mes in view of Zuravleff does not teach the limitations of claims 1 and 13 have been considered but are moot in view of the new grounds of rejection.

STATUS OF CLAIMS IN THE APPLICATION

The following is a summary of the treatment and status of all claims in the application as recommended by **M.P.E.P. ' 707.07(i)**:

CLAIMS REJECTED IN THE APPLICATION

Per the instant office action, claims 1-14 have received a first action on the merits and are subject of a first action non-final after RCE.

DIRECTION OF FUTURE CORRESPONDENCES

Any inquiry concerning this communication or earlier communications from the examiner should be directed to M. Anthony Giardino whose telephone number is (571) 270-3565 and can normally be reached on Monday - Thursday 7:30am - 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mr. Sanjiv Shah can be reached on (571) 272 - 4098. The fax phone

number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

M.A. Giardino

/M.G./

Patent Examiner
Art Unit 2185

February 19, 2010

/Stephen Elmore/
Primary Examiner, Art Unit 2185